

**REMARKS**

Applicant adds claims 81-88. Claims 53-88 are pending in the present application.

The abstract has been objected to. Claims 53-71, 74-76 and 78-79 stand rejected under 35 U.S.C. §112, second paragraph as being indefinite. Claims 53-67 and 73-80 stand rejected under 35 U.S.C. §112, first paragraph as containing subject matter which was not described in the originally filed specification. Claims 53-80 stand rejected under 35 U.S.C. §102(b) for anticipation by U.S. Patent No. 5,475,317 to Smith. Claims 53-80 stand rejected under 35 U.S.C. §102(b) for anticipation by U.S. Patent No. 5,378,311 to Nagayama.

Applicant respectfully traverses the rejections and urges allowance of the present application.

Referring to the prior art rejections, claim 53 stands rejected over Smith and Nagayama. On page 4 of the Action, it is stated that Smith discloses a singulated bare die tester. As set forth in the abstract, Smith discloses a reusable test socket for testing singulated bare die. Smith is related to testing of already fabricated devices including singulated bare die. Smith fails to disclose or suggest positively recited limitations of claim 53. For example, the Smith reference fails to teach or suggest the claimed receiving a wafer within a workpiece processing apparatus and processing the wafer within the workpiece processing apparatus as positively set forth in claim 53. Numerous limitations of claim 53 are not shown or suggested by Smith and claim 53 recites patentable subject matter over Smith for at least these reasons.

Regarding the rejection of claim 53 for anticipation by Nagayama, it is stated that

on page 4 of the Office Action that the holder of Nagayama includes electrical couplings 57-63 for coupling to the wafer. It is further stated that it appears that the wafer inherently has electrical coupling in which the electrical couplings of the holder connected thereto. Nagayama fails to disclose or suggest limitations of claim 53.

As set forth in column 2, line 58 continuing to column 3, line 44 of Nagayama, it is clear that DC power sources 59, 60 are utilized to provide DC power to an electrode 53 *buried within insulation member 52* of chuck 51. RF power source 63 is selectively applied or coupled with wafer stage 55 via a switch 61. Selective application of DC power and RF bias to a chuck in a wafer stage fails to disclose or suggest *communicating signals intermediate circuitry of a wafer and circuitry of a workpiece holder* as recited in claim 53. Furthermore, Nagayama fails to teach or suggest *coupling circuitry of a wafer with circuitry of a workpiece holder*. Wafer 54 of Nagayama is entirely devoid of any circuitry of a wafer or the claimed coupling. Positively recited limitations of claim 53 are not shown or suggested and claim 53 is allowable over Nagayama.

In addition, Applicant objects to the reliance upon inherency set forth in support of the rejection of claim 53 over Nagayama. In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flows from the teachings of the applied prior art. *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). Coupling of circuitry of the wafer is not disclosed or suggested by Nagayama, and does not necessarily flow from the teachings of Nagayama. The Nagayama reference merely discloses a wafer with no teaching or suggestion of the

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claimed coupling circuitry of the wafer with circuitry of the workpiece holder. The reliance upon inherency is misplaced and claim 53 is patentable over Nagayama.

The claims which depend from independent claim 53 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

For example, claim 56 recites altering processing responsive to the communicating. Smith fails to disclose or suggest any processing of a wafer let alone altering of processing of a wafer responsive to communicating signals. Nagayama fails to disclose or suggest any altering of processing responsive to communicating of signals as defined in claim 56. Claim 56 recites limitations not shown or suggested in the art and claim 56 is allowable for least this reason.

Claim 58 recites communicating signals using an intermediate member of the workpiece processing apparatus. No teachings are identified in the Office Action as allegedly corresponding to communication of signals using an intermediate member. Positively recited limitations of claim 58 are not shown or suggested in the art and claim 58 is allowable for at least this reason.

Claim 59 recites contacting circuitry of the wafer and circuitry of the workpiece holder. Smith fails to disclose or suggest wafer teachings, circuitry of a wafer, or contacting circuitry of the wafer with circuitry of a workpiece holder. In addition, Nagayama provides absolutely no teaching or suggestion of contacting circuitry of a wafer with circuitry of the workpiece holder. Further, no teachings are identified in the Office Action as allegedly disclosing or suggesting the claimed contacting. Claim 59 recites limitations not

shown or suggested in the prior art and claim 59 is allowable for at least this reason.

Referring to claim 60, Smith relates to testing of singulated bare die. The abstract of Smith refers to a reusable test socket for testing singulated bare die to determine before packaging that the bare die is a known good die. Smith fails to disclose or suggest any processing of a workpiece within a workpiece processing apparatus to form a semiconductor device and communicating signals intermediate a workpiece and the workpiece processing apparatus as recited in claim 60. Claim 60 recites limitations not shown or suggested in Smith and claim 60 is allowable over Smith for at least this reason.

Nagayama fails to disclose or suggest any communication of signals intermediate the workpiece and the workpiece processing apparatus as recited in claim 60. Application of DC power to a chuck 51 and RF power to chuck 51 fails to disclose or suggest communication of signals intermediate a workpiece and a workpiece processing apparatus as positively recited in claim 60. Claim 60 recites limitations not shown or suggested in the prior art and claim 60 is allowable for at least this reason.

The claims which depend from independent claim 60 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

For example, claim 61 recites *electrically coupling* the workpiece and the workpiece processing apparatus. Nagayama fails to disclose or suggest any electrical coupling of the workpiece and the workpiece processing apparatus. Claim 61 is allowable over Nagayama for at least this additional reason.

Claim 63 recites coupling circuitry of the workpiece and circuitry of the workpiece

holder at a surface of the workpiece and a surface of the workpiece holder. Nagayama fails to disclose or suggest any coupling of circuitry of the workpiece with circuitry of the workpiece holder as recited in claim 63 and claim 63 is allowable over Nagayama for at least this additional reason.

Claim 64 recites receiving the workpiece comprising a semiconductive wafer. Smith clearly pertains to bare die and fails to disclose or suggest receiving a semiconductor wafer within a workpiece processing apparatus. Claim 64 recites limitations not shown or suggested in Smith and claim 64 is allowable over Smith for at least this additional reason.

With respect to claim 68, Smith fails to disclose or suggest supporting a wafer using a workpiece holder as positively recited in claim 68. The bare die of Smith in no fair interpretation discloses or suggests supporting a wafer using a workpiece holder as recited in claim 68. Claim 68 recites limitations not shown or suggested in Smith and claim 68 is allowable over Smith for at least this reason.

Nagayama fails to disclose or suggest coupling circuitry of a wafer with circuitry of a workpiece holder and communicating signals intermediate the circuitry of the wafer and the circuitry of the workpiece holder. Positively limitations of claim 68 are not shown or suggested in Nagayama and claim 68 is allowable over Nagayama for at least reason.

The claims which depend from independent claim 68 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

With respect to claim 73, Smith fails to disclose or suggest providing a workpiece processing apparatus adapted to process a workpiece to form a semiconductive device as

positively recited in claim 73. The apparatus of Smith merely provides testing prior to packaging to determine whether a die is a known good die. Such teachings regarding testing fail to disclose or suggest provision of a workpiece processing apparatus adapted to process a workpiece to form a semiconductor device as positively recited in claim 73. Further, Smith also fails to disclose or suggest providing a workpiece within the workpiece processing apparatus and receiving signals within the workpiece processing apparatus from the workpiece as positively recited in claim 73. Numerous limitations of claim 73 are not shown or suggested in Smith and claim 73 is allowable over Smith for at least these reason.

Nagayama fails to disclose or suggest *communication of signals using a workpiece* and receiving the signals within a workpiece processing apparatus from the workpiece. Application of DC and RF power to a chuck fail to disclose or suggest communication of signals using the workpiece and receiving the signals within the workpiece processing apparatus from the workpiece as specified in claim 73. Numerous limitations of claim 73 are not shown or suggested in Nagayama and claim 73 is allowable over Nagayama for at least these reasons. Applicant respectfully requests allowance of claim 73 in the next Action.

The claims which depend from independent claim 73 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

In the event that a rejection of the claims is maintained with respect to the prior art, or a new rejection made, Applicants respectfully request identification in such asserted

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references of elements which allegedly correspond to limitations of the claims in accordance with 37 C.F.R §1.104(c)(2). In particular, 37 C.F.R §1.104(c)(2) provides that *the pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified*. Further, 37 C.F.R. §1.104(c)(2) states that the Examiner must cite the best references at their command. When a reference is complex or shows or describes inventions other than that claimed by Applicants, the particular teachings relied upon must be designated as nearly as practicable. The pertinence of each reference if not apparent must be clearly explained for each rejected claim specified. Applicants respectfully request clarification of the rejections with respect to specific references and specific references teachings therein pursuant to 37 C.F.R. §1.104(c)(2) in a non-final Action if any claims are not found to be allowable.

Referring to the indefiniteness rejections, on page 2 of the Action, it is stated that it is unclear what "a circuitry of a wafer" represents. Applicant refers to teachings on page 7, lines 12-16 of the originally-filed specification including exemplary embodiments of aspects of the invention wherein electronic device workpieces 20 include semiconductor wafers. Referring to page 10, lines 16-18 of the specification, one exemplary configuration of a workpiece 20 includes circuitry comprising electrical couplings 24, vias 25 and connections 27 corresponding to respective sensors 23. The claimed circuitry of a wafer is definite and understood by one of skill in the art.

Also with reference to claims 53, 68 and 78, it is stated that "a circuitry of the workpiece holder" is allegedly unclear. Once again, Applicant has disclosed exemplary embodiments of the present invention in the detailed description of the preferred

embodiments of the originally- filed application. One example of circuitry of a workpiece holder is described with respect to references 44, 45 of Fig. 2 and on page 9, lines 15-17 of the originally-filed specification. The term is definite to one of skill in the art, the indefiniteness rejection of claims 53, 68 and 78 is inappropriate, and Applicant respectfully requests allowance of claims 53, 68 and 78.

With respect to claims 58, 72 and 79, the Office Action states that it is allegedly unclear what "an intermediate member" represents. Yet again, Applicant refers the Examiner to the originally-filed specification and drawings wherein exemplary embodiments of the invention are disclosed. For example, on page 12, lines 18-22, an exemplary intermediate member 60 is shown with respect to Fig. 3. Claims 58, 72 and 79 are definite and the rejection under §112 is improper.

With respect to claim 60, it is indicated that it is allegedly unclear how the workpiece is processed since there are no specific steps for performing the process. As is clear from the claimed subject matter, Applicant is not claiming specific processing of a workpiece in claim 60 but any processing of the workpiece in combination with the claimed receiving and the communicating. One of skill in the art would understand claim 60 including the defined processing and claim 60 is definite. In addition, the specification includes numerous teachings of processing workpieces and wafers. For example, page two of the application refers to chemically amplified resists which are utilized in deep ultraviolet (DUV) lithography and small micron geometries. Also on page 2, lines 8-12, it is stated that workpiece temperature and workpiece temperature uniformity are parameters which are closely monitored during wafer and workpiece fabrication. As set forth on page 4 of the

specification, exemplary sensors include resistance temperature devices configured to provide process signals containing process information regarding the electronic device workpiece processing apparatus. As set forth on page 2, lines 22-24, temperature sensors across the surface of a wafer are utilized to provide temperature mapping of a workpiece during processing. On page 7, lines 13-19, it is stated that workpieces typically undergo processing from which subsequent devices are formed. Exemplary workpieces include semiconductor wafers, glass or quartz substrates for flat panel or field emission display devices. It is also stated on page 7 that typical production workpieces are processed and subsequently utilized to form products used in a variety of electronic devices. On page 9, lines 4-8, it is stated that process signals provided by sensors 23 and corresponding to processing conditions of workpiece 21 are received within data gathering device 14. Alterations to processing conditions of apparatus 10 can be changed responsive to the reception of the process signals within device 14. On page 16, lines 7-9, it is stated that chuck 40 is isolated to a greater extent from a processing environment utilized to fabricate or process electronic device workpieces. On page 17, lines 3-6, it is stated that one configuration of apparatus 10 of Fig. 6 enables processing of production workpieces while monitoring processing conditions using calibration workpiece 20. Referring to page 19, lines 12-19, it is stated that layer 28 operates to protect surface 21, sensor 23, and electrical connection 27 from the processing environment including gases, chemicals, plasmas, etc. utilized during processing of electronic device workpieces. The language of processing the workpiece within the workpiece processing apparatus to form a semiconductor device is definite and in compliance with 35 U.S.C. §112, second

paragraph. One of skill in the art would understand limitations of claim 60 especially in consideration of the numerous teachings of the originally filed specification. Applicant respectfully requests withdrawal of the indefiniteness rejection of claim 60.

Regarding claims 62, 68, and 74 and referring to page 10, lines 16-18 of the specification, one exemplary configuration of a workpiece 20 includes circuitry comprising electrical couplings 24, vias 25 and connections 27 corresponding to respective sensors 23. The claimed "circuitry of a workpiece" is definite and understood by one of skill in the art.

With reference to claims 62 and 74 and "a circuitry of the apparatus" language, Applicant refers the Examiner again to exemplary embodiments described in the originally filed specification wherein apparatus 10 in one configuration includes a workpiece holder 12. Circuitry of workpiece holder 12 (and apparatus 10) are shown in one example with respect to references 44, 45 of Fig. 2 and on page 9, lines 15-17 of the originally-filed specification.

Regarding claims 54, 63, 70 and 78, Applicant has deleted the "interface" language without admitting to the propriety of the indefiniteness rejections with respect to such claims.

Referring to the 35 U.S.C. §112, first paragraph rejections, it is stated that apparently, the specification does not have support for limitations of claims 53, 60 and 73. As identified above, the originally filed specification is replete with teachings of processing a workpiece, such as a wafer, within a workpiece processing apparatus to form at least one semiconductor device, processing a workpiece within the workpiece processing apparatus

to form a semiconductor device and providing a workpiece processing apparatus (see reference 10 of the originally-filed specification) adapted to process a workpiece to form a semiconductor device. The disclosure of the originally filed specification provides support for the claimed subject matter especially with reference to the disclosed exemplary embodiments of electronic device workpiece processing apparatus 10 and processing of workpieces 20 as described in the originally filed specification. In addition, Applicant refers the Examiner to U.S. Patent Application Serial No. 09/032,184 incorporated into the subject application by reference as set forth on page 3, lines 9-15 of the originally filed specification. Serial No. 09/032,184 includes additional teachings providing support for claims 53, 60, 73. Applicant respectfully requests of the withdrawal of the 35 U.S.C. §112, first paragraph rejection of claims 53-67 and 73-80.

Applicant has amended the abstract as indicated herein.

Applicant submits an Information Disclosure Statement herewith.

Applicant encloses copies of forms PTO-1449 which include references which have not been initialed by the Examiner. Applicant respectfully requests initialization of reference AE on the form PTO-1449 submitted 4/02/01, initialization of all references upon the forms PTO-1449 submitted 11/5/01 and 1/5/02 and forwarding copies of the initialed forms to Applicant.

Applicant respectfully requests allowance of all pending claims.

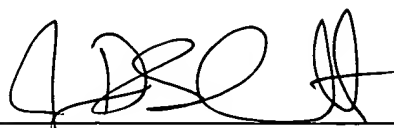
The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

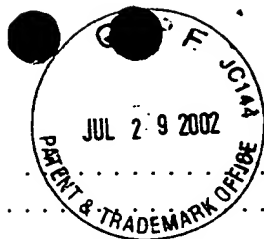
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Appl. No. 09/827,248

Respectfully submitted,

Dated: 7/29/02

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Application Serial No. 09/827,248  
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Inventor David R. Hembree  
Assignee Micron Technology, Inc.  
Group Art Unit 2829  
Examiner V. Nguyen  
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VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING  
RESPONSE TO MARCH 27, 2002 OFFICE ACTION

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In the Abstract

The abstract has been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

~~The present invention includes an~~ An electronic device workpiece processing apparatus and method of communicating signals within an electronic device workpiece processing apparatus are provided. One embodiment of an electronic device workpiece processing apparatus includes a chuck including a surface, an electrical coupling adjacent the surface, and electrical interconnect configured to connect with the electrical coupling of the chuck and conduct a signal within the chuck; an intermediate member having a first surface and a second surface and the intermediate member including: an electrical coupling adjacent the first surface and configured to couple with the electrical coupling of the chuck; an electrical coupling adjacent the second surface; and an electrical interconnect configured to connect the electrical coupling adjacent the first surface and the electrical coupling adjacent the second surface; and an electronic device workpiece

configured to couple with the second surface of the intermediate member, the electronic device workpiece including a sensor and an electrical coupling configured to provide electrical connection of the sensor with the electrical coupling of the second surface of the intermediate member.

#### In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

54. (Amended) The method in accordance with claim 53 wherein the coupling comprises coupling the circuitry of the wafer and the circuitry of the workpiece holder at ~~an interface of~~ a surface of the wafer and a surface of the workpiece holder.

63. (Amended) The method in accordance with claim 60 further comprising:  
supporting a workpiece using a workpiece holder of the workpiece processing apparatus; and  
coupling circuitry of the workpiece and circuitry of the workpiece holder at ~~an interface of~~ a surface of the workpiece and a surface of the workpiece holder.

70. (Amended) The method in accordance with claim 68 wherein the coupling comprises coupling the circuitry of the wafer and the circuitry of the workpiece holder at ~~an interface of~~ a surface of the wafer and a surface of the workpiece holder.

78. (Amended) The method in accordance with claim 77 further comprising coupling circuitry of the workpiece and circuitry of the workpiece holder at ~~an interface of~~ a surface of the workpiece and a surface of the workpiece holder.

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